

## Prior Art

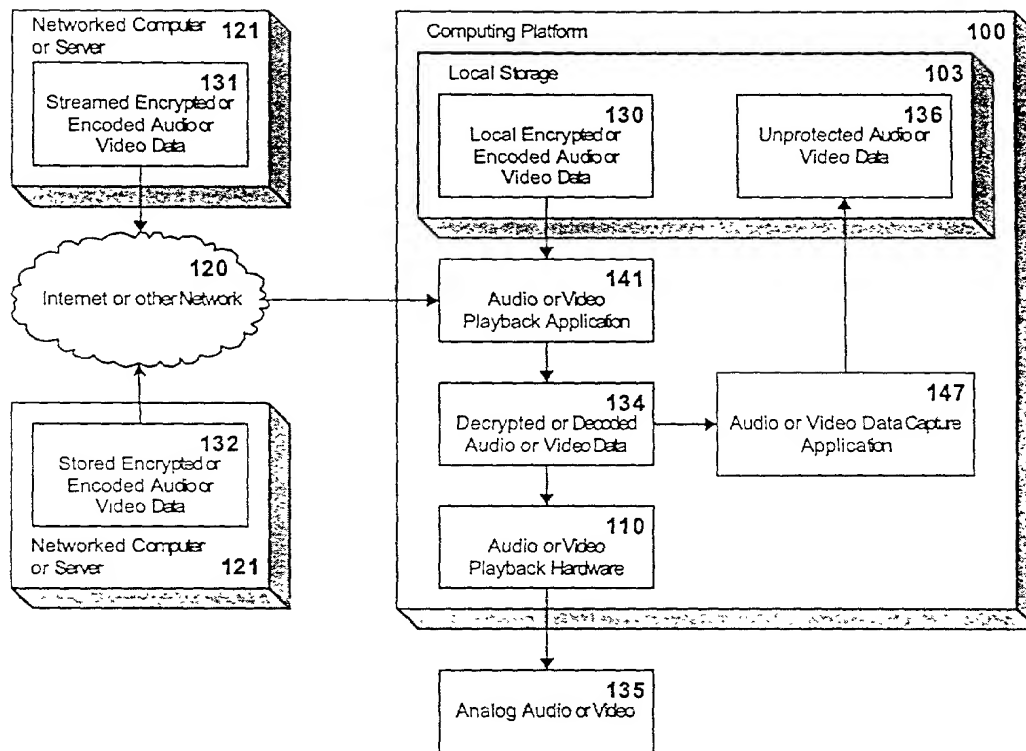


Figure 1

# Prior Art

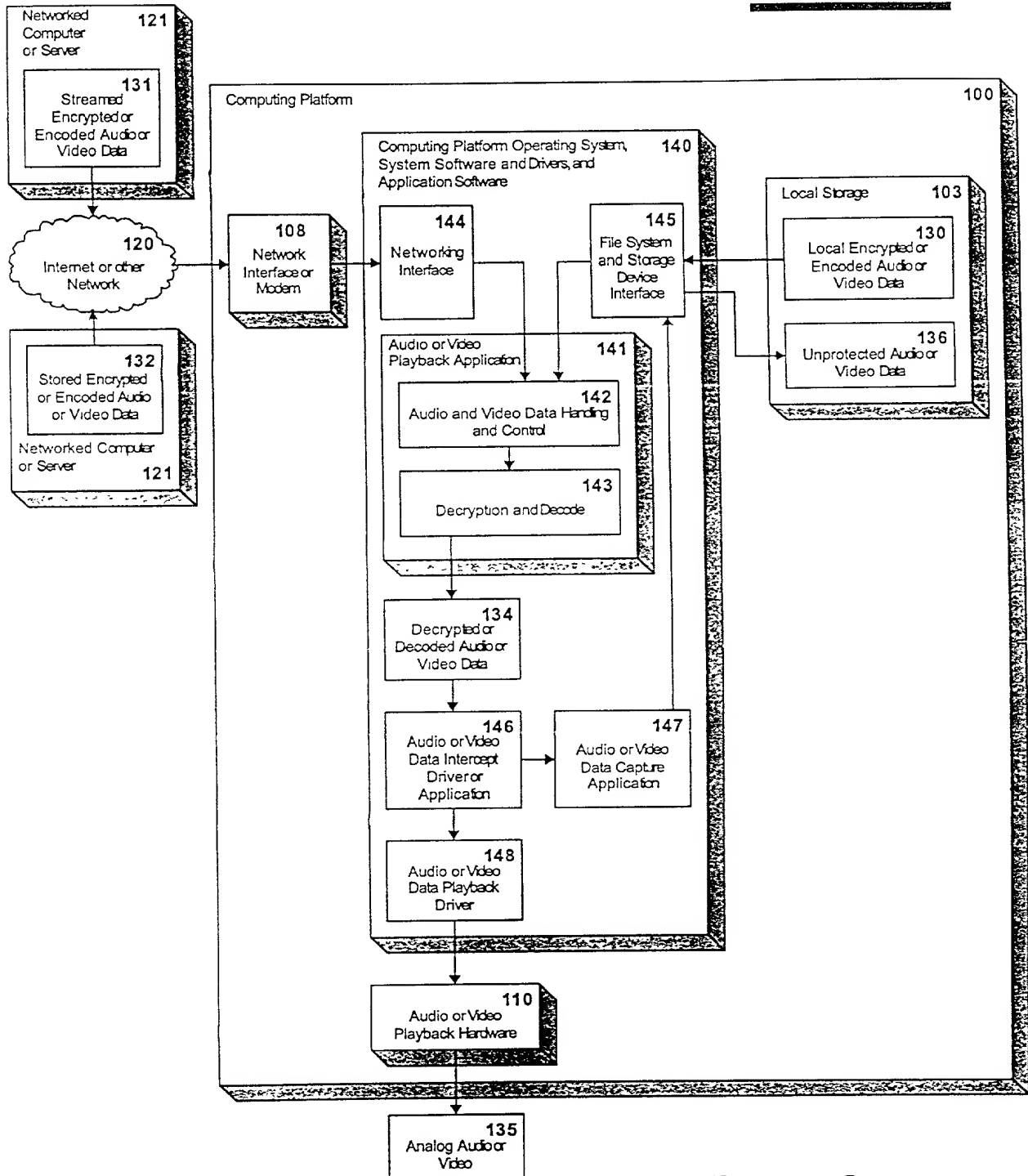
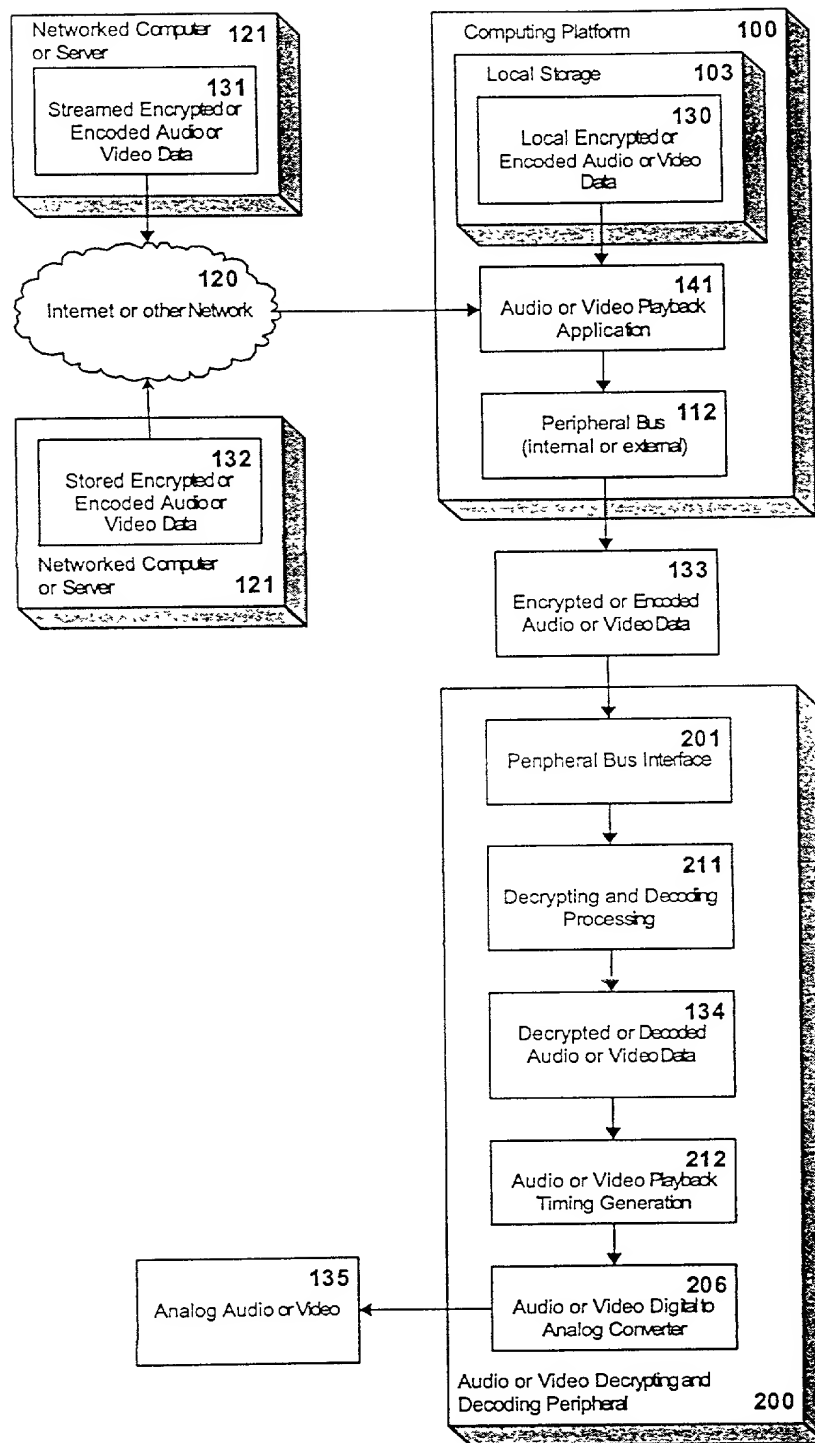
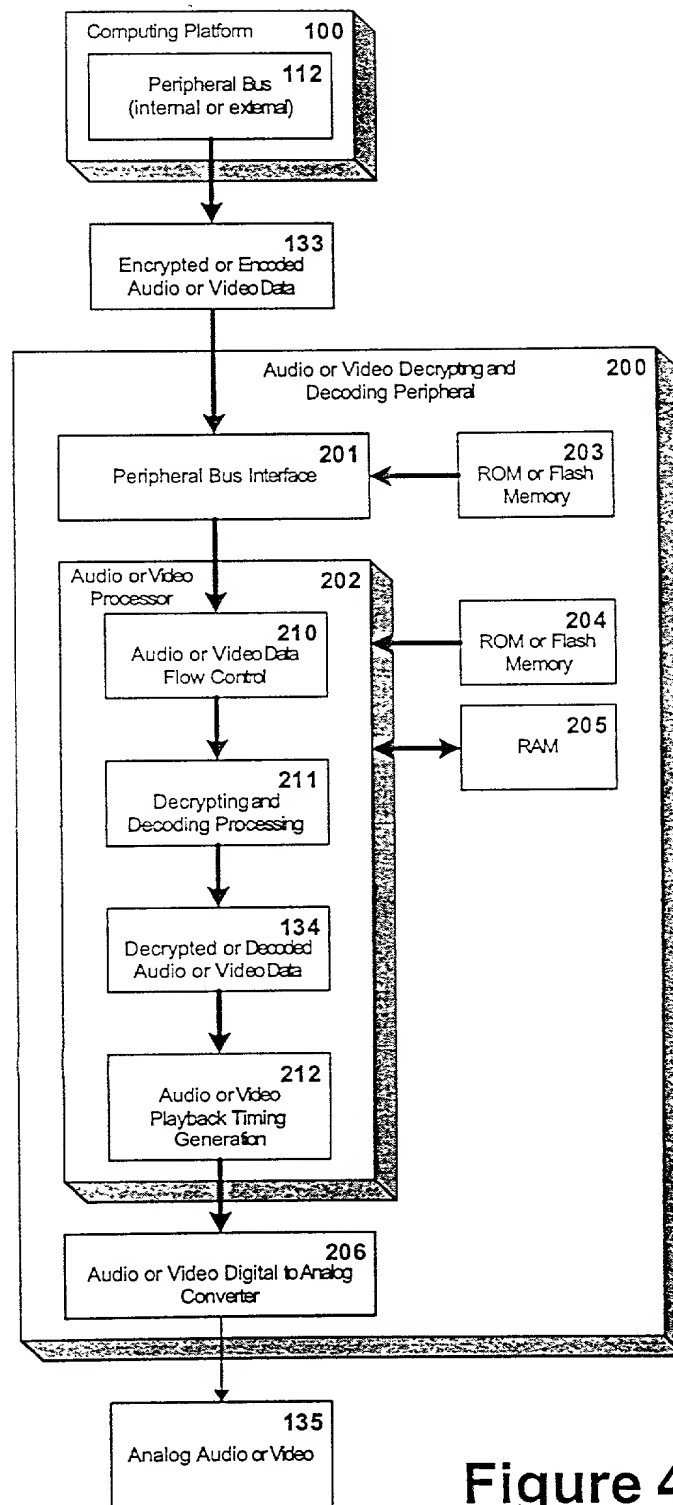


Figure 2



**Figure 3**



**Figure 4**

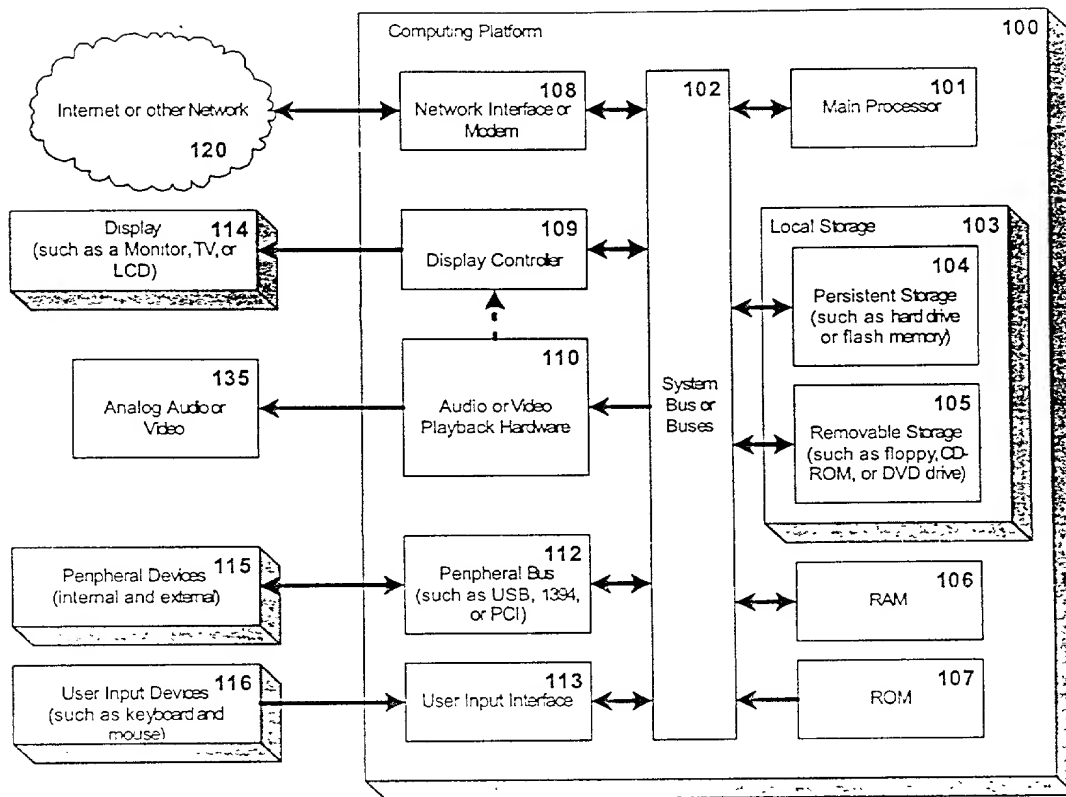


Figure 5

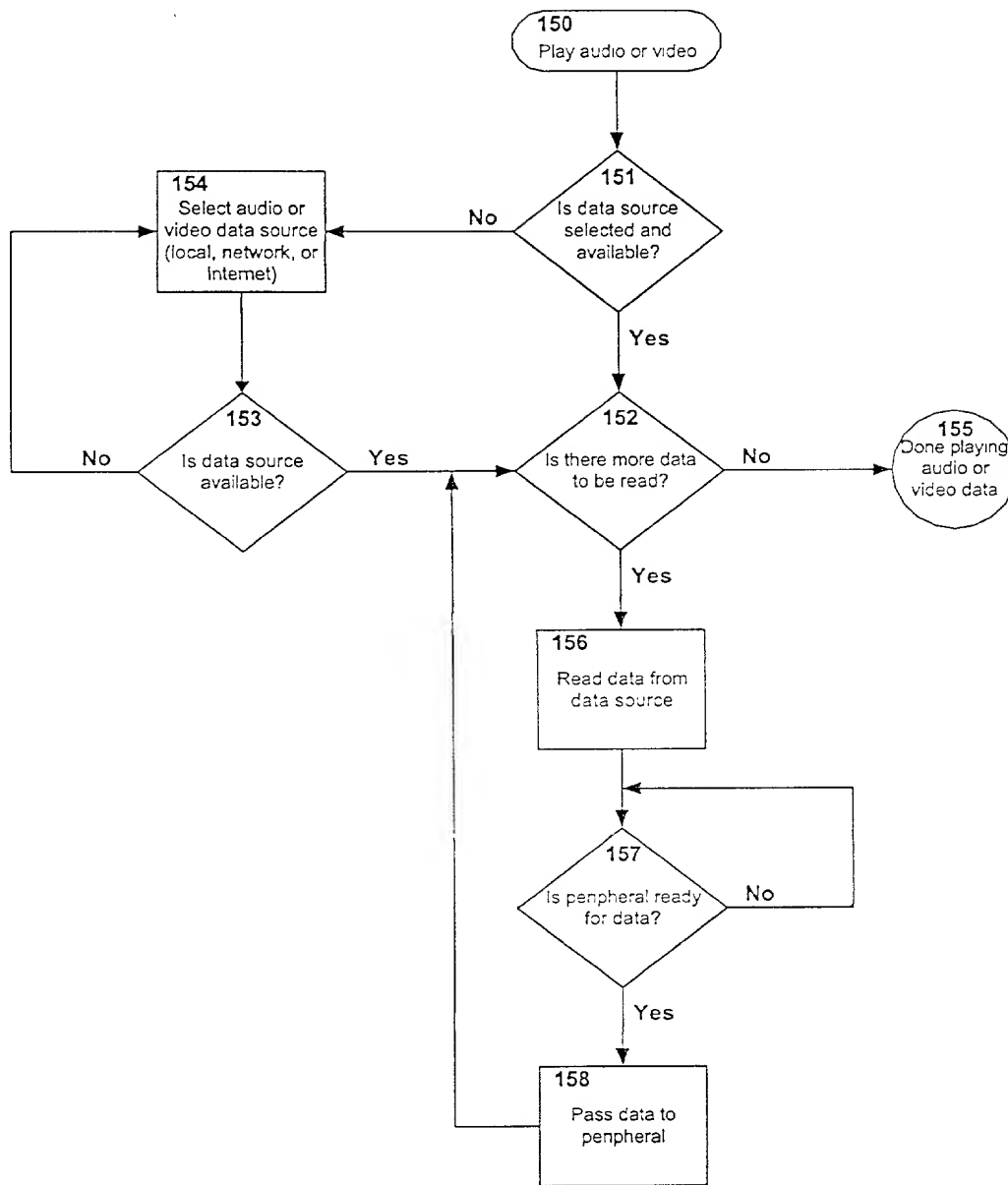


Figure 6

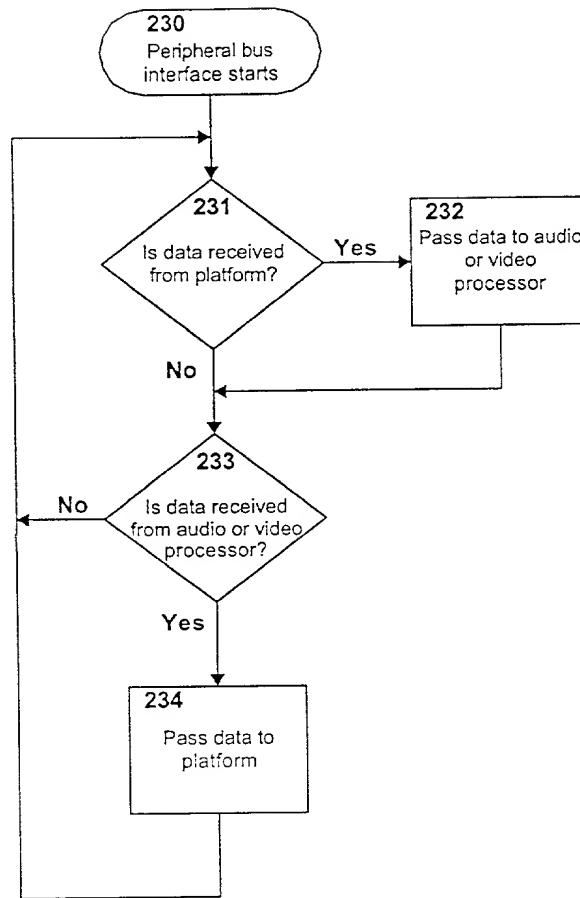
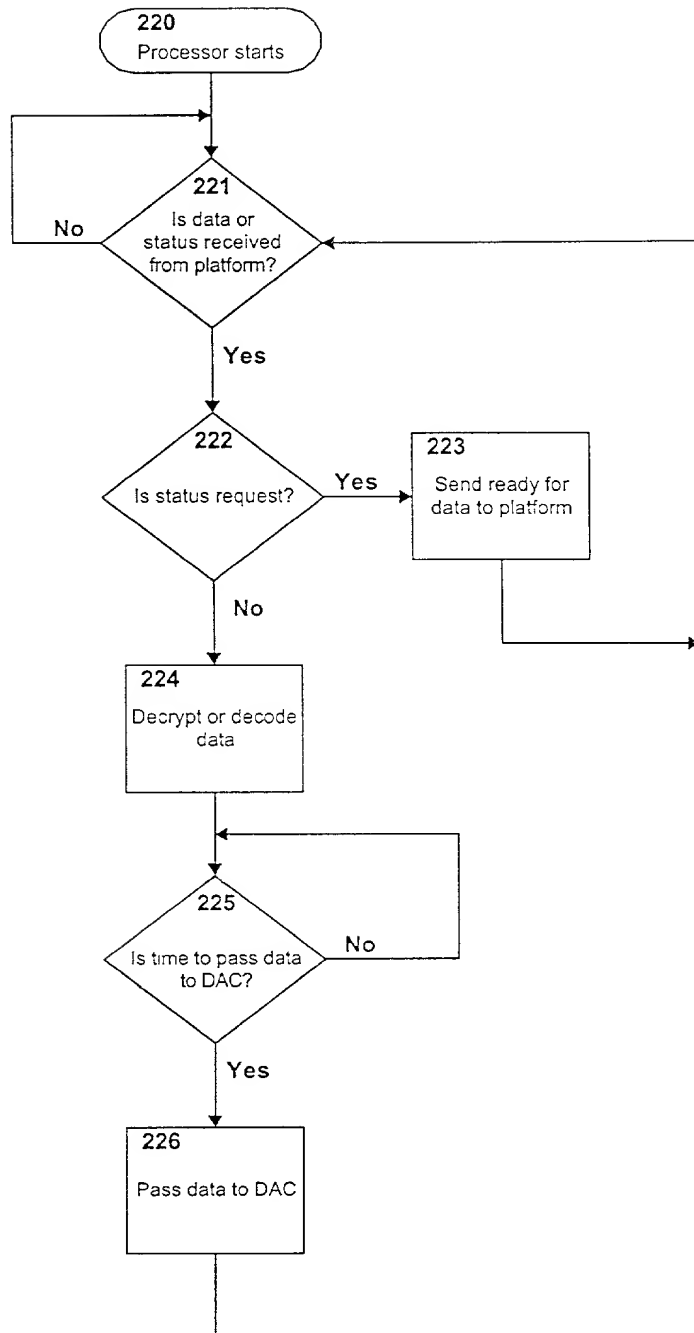


Figure 7



**Figure 8**



Figure 9 shows the schematic diagram of the system. The diagram illustrates the interconnection of various components, including the DSP, memory, and peripheral devices, through a central bus system.

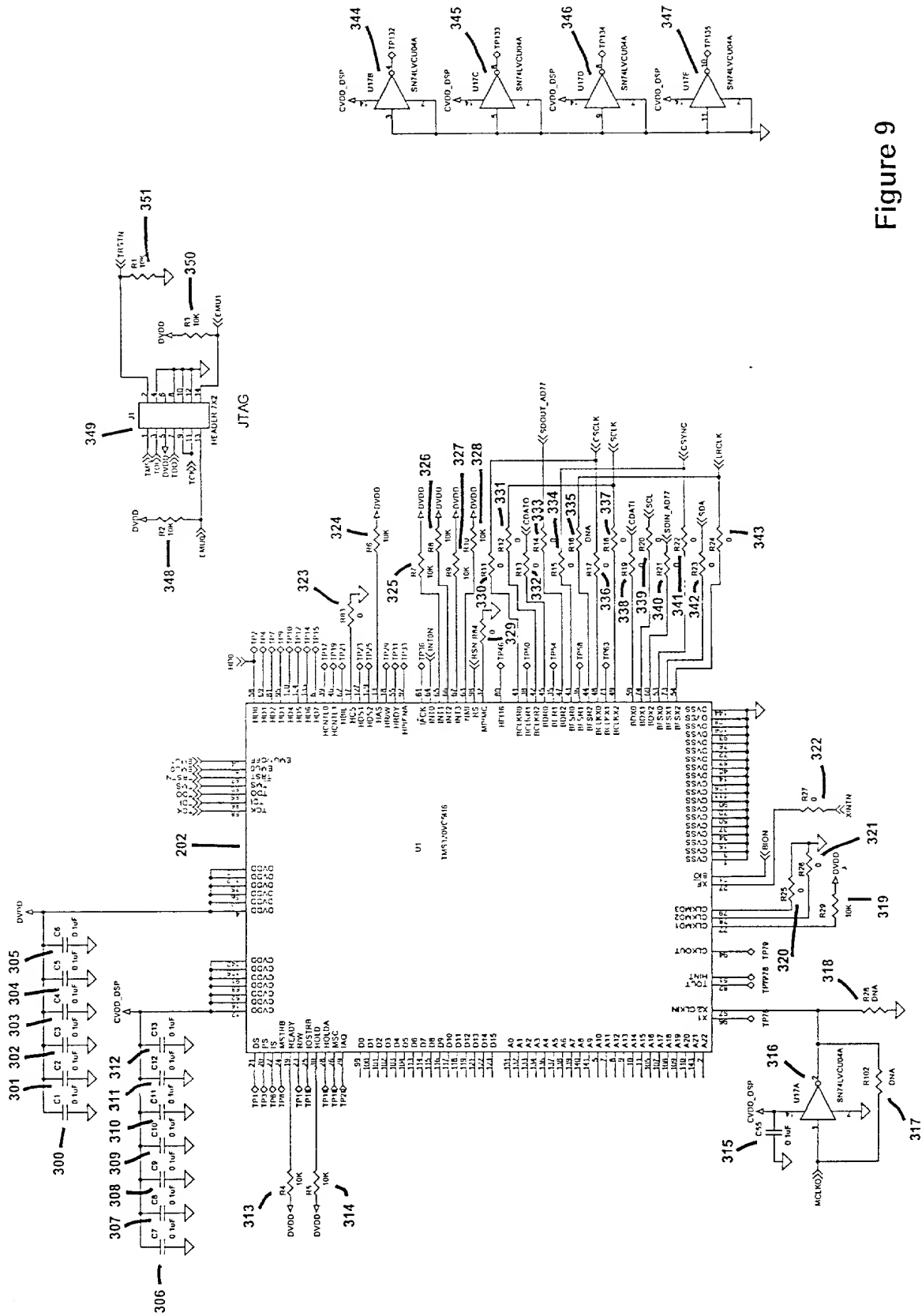


Figure 9

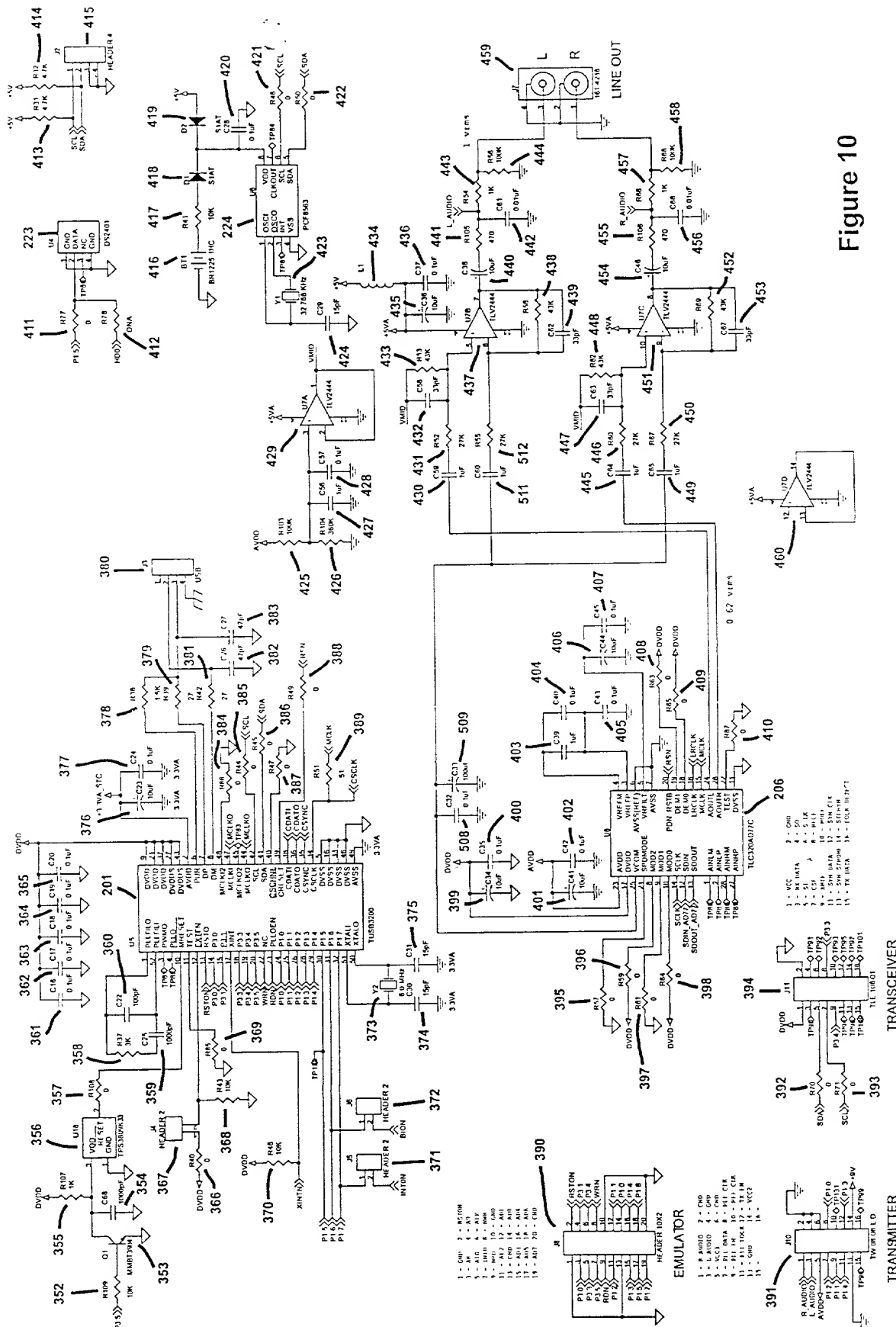
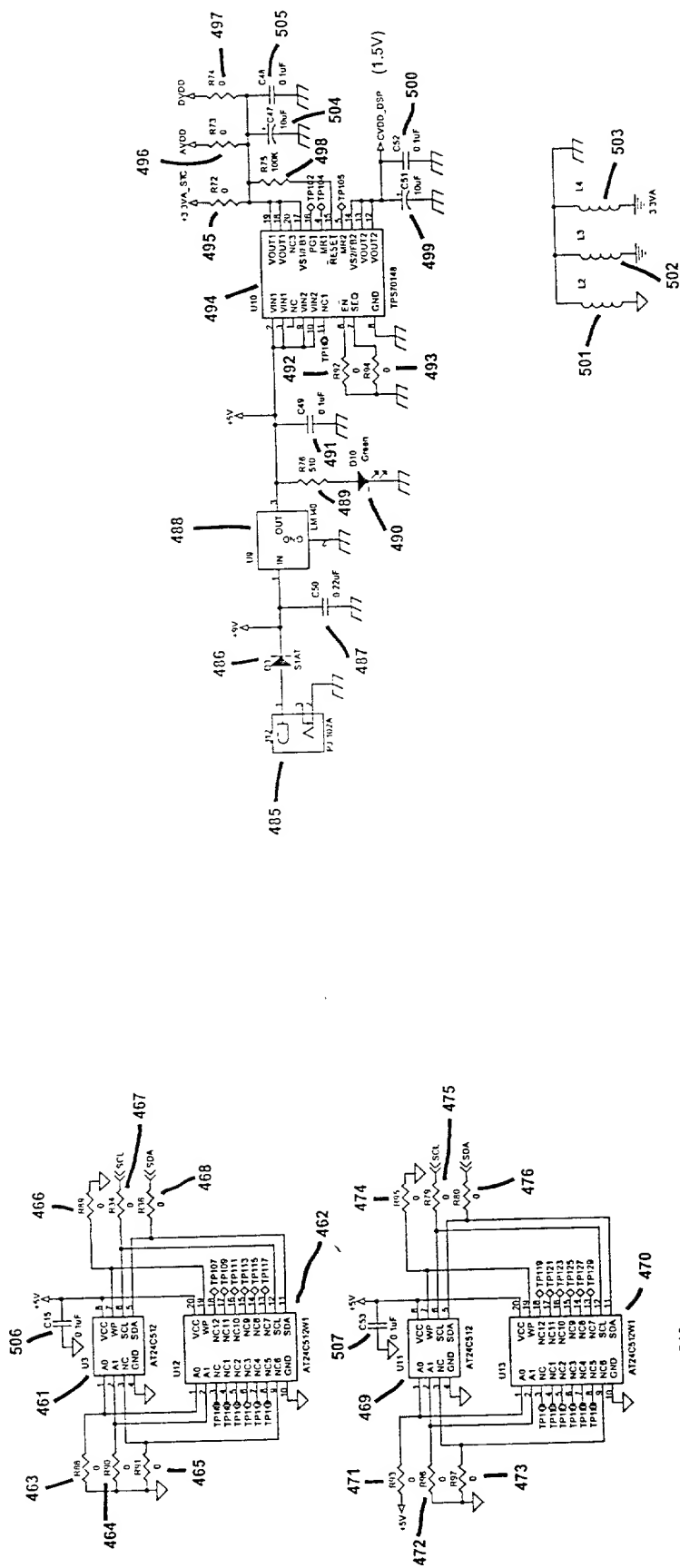


Figure 10



**Figure 11**